

AMENDMENTS TO THE ABSTRACT

Please cancel the Abstract section of the specification and replace with the following:

ABSTRACT

Apparatus for testing a system on a chip (SOC) comprises a first SOC including a first hard disk controller and a first read channel. A second SOC comprises a second hard disk controller and a second read channel. An arbitrary waveform generator (AWG) generates a timing signal. An adder is provided in communication with the arbitrary waveform generator. The first SOC differentiates the timing signal received from the arbitrary waveform generator and generates a write signal in synchronization with the timing signal. The adder adds the write signal from the first SOC and the timing signal to output a combined signal having a timing signal component and a write signal component. The second SOC differentiates the timing signal component which simulates a servo signal and the write signal component simulates a signal being accessed by a read channel.